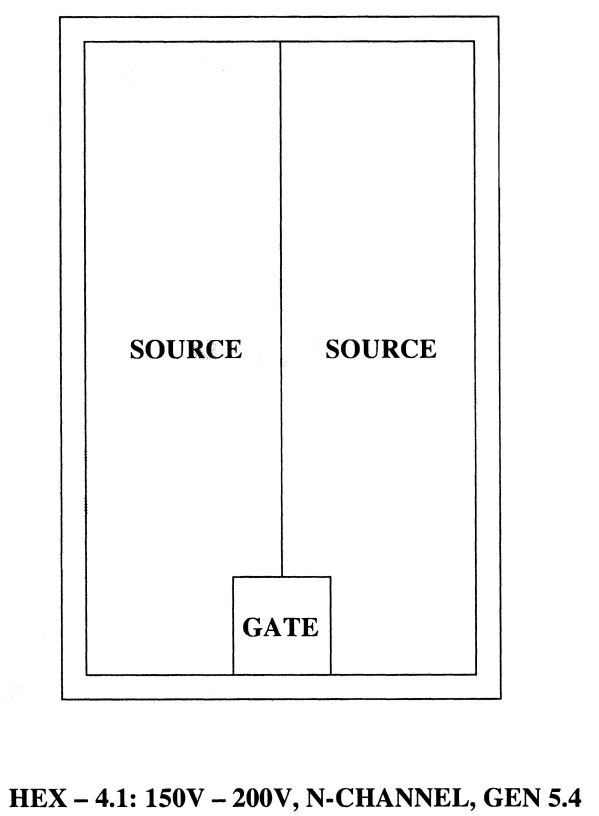
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: G = .021” X .022”**

**Backside Potential: DRAIN**

**Mask Ref: GEN 5.4**

**APPROVED BY: DK DIE SIZE .165” X .248” DATE: 7/11/22**

**MFG: IR THICKNESS .010” P/N: IRFC52N15DB**

**DG 10.1.2**

#### Rev B, 7/19/02